REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Drawings

The drawings have been objected to as not showing a "bridge". However, it is respectfully submitted that Fig. 1 illustrates bridge 170 that connects fill bus 135 to DMA bus 145 via multiplexer 175. Accordingly, it is respectfully requested that this objection be withdrawn.

35 USC § 102 / 35 USC § 103

Claims 1-8, 10-22, and 24-32 have been rejected under 35 USC § 102(e) as allegedly being anticipated by Wakimoto. Claims 22 and 24-28 have been rejected under 35 USC § 103(a) as allegedly being unpatentable over Wakimoto. These rejections are respectfully traversed.

Claim 1 defines a method comprising routing a memory access from a processor core back into the processor core through a bus interface coupled to the processor core without traversing memory external to the processor core.

Claim 8 defines, inter alia, a multiplexing unit operative to switch between the second bus and the bridge to enable information placed onto the first bus to be re-routed into the second port without traversing memory external to the processor core.

Claim 15 defines, inter alia, a machine to route a memory access from a processor core back into the processor core

through a bus interface coupled to the processor core without traversing memory external to the processor core.

Claim 22 defines, inter alia, a multiplexing unit operative to switch between the second bus and the bridge to enable information placed onto the first bus to be re-routed into the second port without traversing memory external to the processor.

Claim 30 defines, inter alia, a processor connected to the bus interface, the processor being operative to reroute a memory access from the processor back into the processor through the bus interface without traversing memory external to the processor.

Wakimoto illustrates and describes an arrangement in which a core is coupled to a local memory 3 external to a microprocessor 1 via a bus (not numbered). The local memory 3 is coupled to a main memory 2 (also external to the microprocessor 1) via an external bus 43. The main memory 2 in turn is coupled to an instruction cache 12 via an external bus 41. The microprocessor is connected to a peripheral circuit (not shown) via the external bus 41, the bus bridge 5, and an external bus 44. No further details regarding the bus bridge 5 are provided.

Wakimoto fails to disclose, as defined in the various claims, routing a memory access from a processor core back into the processor core through a bus interface coupled to the processor core. In particular, Wakimoto fails to disclose routing a memory access without traversing memory external to the processor core.

Wakimoto does not suggest memory access being routed from a processor core back into the processor core. Even if Wakimoto did suggest it, however, the access would be routed to the local

memory 3 and then to the bus bridge 5 via the external bus 43. From the bus bridge 5, the external bus 41 would then be used to route the memory access back to the microprocessor 1. This would require traversing local memory 3. Therefore, Wakimoto does not anticipate the claimed subject matter.

Accordingly, all of the claims should be allowable.

Allowed Claims

The indication that claims 9 and 23, inter alia, would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims is appreciatively noted. These claims have been rewritten as new claims 33 and 34.

Concluding Comments

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply charges related to the extra claim fees and the Petition for Extension of Time and any other charges or credits to deposit account 06-1050.

Attorney's Docket No.: 10559-567001 / P12729

Respectfully submitted,

Date: 1/27/05

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